REMARKS

Reconsideration of the above-identified application is respectfully requested. Claims 1-11 remain in this application. The specification has been amended to clarify that the field oxide region behaves qualitatively like a second transistor. Support for the amendment can be found on page 6, lines 12-15; no new matter has been added. Attached hereto is a marked-up version of the changes made to the drawings and specification by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

I. Drawings

The drawing correction filed on June 27, 2002 was disapproved since numeral 24 was not identified in the specification and two or more FETs on said substrate were not shown. Applicants have attached new Fig. 1, which clearly shows two FETs (indicated by numeral 12). Additionally, the specification has been amended to reference numeral 24 as the isolation region.

II. Rejection under 35 U.S.C. § 103

Claims 1-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,274,914 to Park et al. in view of U.S. Patent 5,289,027 to Terrill et al. The Examiner noted that Park does not disclose a negative voltage source for applying a steady back bias to a NMOS region of said substrate to increase the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in said field oxide region thereby mitigating total dose radiation effects. Therefore, the Examiner supplemented Park with Terrill's negative voltage source for applying a steady back bias.

Applicants respectfully submit that claims 1-11 are not obvious over Park et al. in view of Terrill et al. It is well settled that "obviousness cannot be established by combining the teachings

of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." *In re Geiger*, 815 F.2d 686, 688, 2 U.S.P.Q.2d 1276, 1278 (Fed. Cir. 1987). To establish a prima facie case of obviousness, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (C.C.P.A. 1979); M.P.E.P. 2143.03.

In the present invention, a back bias is applied to a bulk CMOS device to shut off radiation-induced leakage currents in the field oxide while still allowing the device to operate within its operational range. Park discloses a bulk CMOS device, but does not disclose a steady negative voltage source for applying a steady back bias. Terrill discloses applying a back bias to a SOI CMOS to avoid punchthrough and other short-channel effects. Terrill does not discuss the problem of radiation in CMOS devices; the only mention of radiation by Terrill is that the SIMOX "technique has been used to improve radiation hardness." (Col. 1, lines 17-25). Moreover, Terrill does not discuss charge build up in the field oxide and specifically states that the "applied back-gate bias produces an electric field which induces charged carriers **in the channel region**." (Col. 3, lines 37-39, emphasis added). Thus, neither Terrill nor Park disclose "a negative voltage source for applying a steady negative back bias to a NMOS region of said substrate to increase the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in said field oxide region thereby mitigating total dose radiation effects" as described in independent claims 1 and 7 of the present application.

Since the combination of Park and Terrill does not teach or suggest every element of independent claims 1 and 7, Applicants respectfully submit that claims 1-11 (claims 2-6 are

dependent on claim 1 and claims 8-11 are dependent on claim 7) are not obvious over Park in view of Terrill.

In view of the foregoing, it is respectfully submitted that this application is ready for allowance. Applicants respectfully request that the Examiner withdraw the outstanding rejection and allow this application to issue.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 50-0281.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Drawings:

New Fig. 1 has been attached hereto.

In the Specification:

The paragraph beginning at page 5, line 6, has been amended as follows:

The negative bias source 22 is adapted for applying a steady negative back bias to the substrate at a voltage that mitigates total dose radiation failures. The device operates by mitigating leakage currents about the device, while allowing the device to operate within its operational range, i.e., without changing the threshold voltage of the device to a degree that will cause the device to operate poorly. Typically, this negative bias will be between about –3 V and about –0.5 V, relative to the source. The inventors have recognized that in the current generation of commercial CMOS devices, total dose radiation failures arise in the isolation region 24 rather than in the gate region.

The paragraph beginning at page 5, line 13, has been amended as follows:

Without wishing to be bound by theory, the inventors propose that the reason this method works is that the negative bias raises the threshold voltage in the field (isolation) region and therefore tends to shut off radiation-induced parasitic leakage currents. The field oxide region behaves qualitatively like a second transistor in parallel to the intended transistor and has its own effective threshold voltage that is more strongly affected by the back bias. Larger negative biases will make the devices harder against total dose radiation. However, higher biases will also tend to shift the gate threshold voltage for the FETs in the CMOS device. To compensate for this, the device will typically be engineered so that the threshold voltage is within a preferred operational

range (typically between about 0.4 V and about 0.6 V for a device operating at 3 V) when this back bias is applied. However, the method will work for other conditions. For example, it is especially effective with even lower thresholds.